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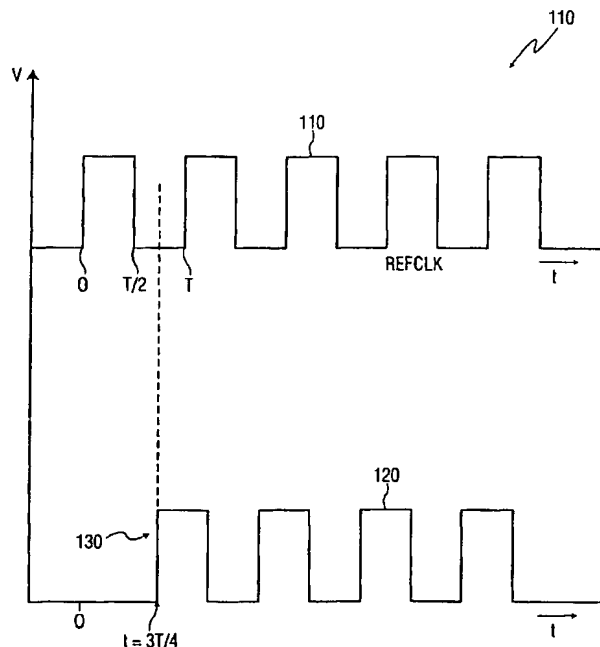
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- Declaration under Rule 4.17:**
— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for all designations

[Continued on next page]

(54) Title: COARSE DELAY TUNER CIRCUITS WITH EDGE SUPPRESSORS IN DELAY LOCKED LOOPS



(57) Abstract: The invention discloses a delay locked loop which includes a coarse delay tuner circuit with edge suppressors suitable for use with delay locked loops (DLLs). The disclosed tuner circuit provides reduced lock time of the DLL circuit.

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 304 116 B1 (YOO CHANG-SIK ET AL) 16 October 2001 (2001-10-16) column 6, line 44 - column 7, line 15	1-31
A	US 6 215 726 B1 (KUBO TAKASHI) 10 April 2001 (2001-04-10) column 8, line 39 - column 10, line 29	1-31
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 08, 30 June 1999 (1999-06-30) & JP 11 085308 A (NIPPON STEEL CORP), 30 March 1999 (1999-03-30) abstract; figure 3	1-31

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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